

MAR 30 2004

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of

Masahiro Shimada, et al.

Serial No.: 10/747,807

Group Art Unit: Not Yet Assigned

Filing Date: December 30, 2003

Examiner: Unknown

For: **WIRING STRUCTURE FOR SEMICONDUCTOR DEVICE**

Honorable Commissioner of Patents  
Alexandria, Virginia 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. Copies of the listed documents are provided herewith for the convenience of the Examiner. In compliance with the concise explanation requirement under 37 CFR §1.98(a)(3), the relevance of these documents is discussed on page 2 of the subject application.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-0481.

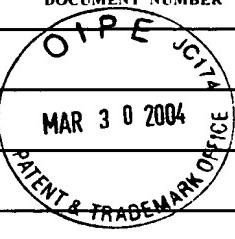
Respectfully submitted,



Sean M. McGinn  
Registration No. 34,386

Date: 3/30/04

McGinn & Gibb, PLLC  
Intellectual Property Law  
8321 Old Courthouse Road, Suite 200  
Vienna, VA 22182-3817  
(703) 761-4100  
Customer No. 21254

<b>INFORMATION DISCLOSURE CITATION</b> <i>(Use several sheets if necessary)</i>				Docket Number (Optional) <b>PTGF-03070</b>		Application Number <b>10/747,807</b>	
				Applicant(s) <b>Masahiro SHIMADA, et al.</b>			
				Filing Date <b>December 30, 2003</b>	Group Art Unit <b>Not Yet Assigned</b>		
U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
							
FOREIGN PATENT DOCUMENTS							
REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)							
		Kazuhide Abe, et al., "High Reliable Cu Damascene Interconnects with Cu/Ti/TiN/Ti Layered Structure", Oki Technical Review, No. 184, Vol. 67, No. 3, pp. 65-68, October 2000.					
		Miki Moriyama, et al., "Future Fabrication Techniques for Cu Wires used in Si ULSI Devices", Material Japan, Vol. 39, No. 11, pp. 901-908 (2000).					
EXAMINER				DATE CONSIDERED			